

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
						M-11822 US		09/925,102	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)			
(Use several sheets if necessary)						Jack H. Yuan et al.			
COPY						Filing Date		Group	
						August 8, 2001		2003	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
IA	AA	5,043,940	Aug. 27, 1991	Harari	_____	_____			
	AB	5,070,032	Dec. 3, 1991	Yuan et al.	_____	_____			
	AC	5,095,344	Mar. 10, 1992	Harari	_____	_____			
	AD	5,172,338	Dec. 15, 1992	Mehrotra et al.	_____	_____			
	AE	5,297,148	Mar. 22, 1994	Harari et al.	_____	_____			
	AF	5,313,421	May 17, 1994	Guterman et al.	_____	_____			
	AG	5,315,541	May 24, 1994	Harari et al.	_____	_____			
	AH	5,343,063	Aug. 30, 1994	Yuan et al.	_____	_____			
	AI	5,661,053	Aug. 26, 1997	Yuan	_____	_____			
	AJ	5,712,180	Jan. 27, 1998	Guterman et al.	_____	_____			
IA	AK	6,103,573	Aug. 15, 2000	Harari et al.	_____	_____			
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
IA	AL	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.							
	AM	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.							
	AN	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.							
IA	AO	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.							
Examiner		Date Considered							
Angela		6/24/04							
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
<u>IA</u>	AP	6,151,248	Nov. 21, 2000	Harari et al.	—	—			
<u>IA</u>	AQ	6,222,762	Apr. 24, 2001	Guterman et al.	—	—			
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		Document	Date	Country	Class	Subclass	Yes	No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
<u>IA</u>	AR	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.							
	AS	Eitan et al., "NR0M: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.							
	AT	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.							
<u>IA</u>	AU	Hori et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," <i>IEDM</i> 92, April 1992, pp. 469-472.							
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U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.257US0		09/925,102	
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Jack H. Yuan et al.							
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	AC	6,103,573	08/15/2000	Harari	—	—	
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JA	AE	6,518,618	02/11/2003	Fazio	—	—	

U.S. Published Patent Application Documents							
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JA	AG	WO 01/41199	07.06.2001	PCT	—	—	Yes	No
	AH	EP 0 780 902 A1	25.06.1997	EP	—	—		
JA	AI	EP 1 104 023 A1	30.05.2001	EP	—	—		

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Examiner <u>Agarwal</u>	Date Considered <u>6/24/04</u>
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JA	AA	6,281,075	Aug. 28, 2001	Yuan et al.	—	—	
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Examiner <i>Angela</i>		Date Considered <i>6/24/04</i>					
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